The Invention Claimed Is:

1. A method of fabricating an integrated circuit having conductor layers separated by insulating layers arranged substantially parallel to a plane of the integrated circuit, comprising:

forming an inductor within the conductor layers and the insulating layers and having magnetic flux lines substantially parallel to the plane of the integrated circuit upon operation of the integrated circuit.

2. A method as defined in claim 1 wherein:

the step of forming the inductor further comprises:

forming the inductor in a substantially coil-shaped configuration.

3. A method as defined in claim 1 wherein:

the step of forming the inductor further comprises:

forming a first segment of the inductor;

forming a second segment of the inductor proximate to and spaced apart from the first segment; and

electrically connecting the first segment and the second segment.

4. A method as defined in claim 3 wherein:

the step of forming the first segment further comprises:

forming the first segment of the inductor having a coil-shape in a first spiraling angular direction; and

the step of forming the second segment further comprises:

forming the second segment of the inductor having a coil-shape in a second spiraling angular direction.

5. A method as defined in claim 3 wherein:

the step of forming the first segment further comprises:

forming the first segment of the inductor having a magnetic flux field in a predetermined orientation upon operation of the integrated circuit; and

the step of forming the second segment further comprises:

forming the second segment of the inductor having a magnetic flux field in the predetermined orientation upon operation of the integrated circuit.

6. A method as defined in claim 3 wherein the integrated circuit includes other components for performing functions of the integrated circuit, further comprising:

forming conductors between the first segment and the second segment, the conductors electrically connecting the other components of the integrated circuit.

7. A method as defined in claim 3 wherein:

the step of electrically connecting the first segment and the second segment further comprises:

forming an electrical conductor in only one of the conductor layers between the first segment and the second segment.

8. A method as defined in claim 1 wherein:

the step of forming the inductor further comprises:

forming a plurality of segments of the inductor; and

electrically connecting the segments.

9. A method as defined in claim 1 wherein:

the inductor includes an end;

the integrated circuit includes an edge; and

the step of forming the inductor further comprises:

forming the inductor with the end thereof proximate to the edge of the integrated circuit.

10. A method as defined in claim 9 wherein:

the aforementioned edge of the integrated circuit is a first edge;

the integrated circuit includes a second edge opposite the first edge;

the aforementioned end of the inductor is a first end;

the inductor includes a second end opposite the first end; and

the step of forming the inductor further comprises:

forming the inductor with the first end thereof proximate to the first edge of the integrated circuit and the second end of the inductor proximate to the second edge of the integrated circuit.

11. A method as defined in claim 9 wherein:

the magnetic flux lines of the inductor have a greatest density at the end of the inductor proximate to the edge of the integrated circuit upon operation of the integrated circuit.

12. A method as defined in claim 1 wherein the inductor has a substantially rectangular cross section and includes horizontal legs and vertical legs, further comprising:

forming the horizontal legs within the conductor layers; and

forming the vertical legs within the conductor layers and the insulating layers.

13. A method as defined in claim 1 wherein the aforementioned inductor is a first inductor, further comprising:

forming a second inductor within the conductor layers and the insulating layers and having magnetic flux lines substantially parallel to the plane of the integrated circuit upon operation of the integrated circuit, the second inductor being substantially similar to the first inductor and offset laterally and longitudinally from the first inductor.

14. A method as defined in claim 1 wherein the aforementioned inductor is a first inductor, further comprising:

forming a plurality of inductors similar to the first inductor, each of the inductors having an inductance;

electrically connecting the inductors in a series in which each inductor, except a last inductor in the series, is followed by at least one inductor subsequent thereto and each inductor, except an initial inductor in the series, is preceded by at least one inductor;

electrically connecting the inductors with a plurality of switch devices, each switch device corresponding to at least one of the inductors, each switch device turning off the corresponding inductor and any inductors subsequent to the corresponding inductor when the switch device is in a first state, each switch device turning on the corresponding inductor when the switch device and the switch

devices corresponding to any inductors preceding the corresponding inductor are in a second state, each of the inductors adding to an over-all inductance of the plurality of inductors when turned on;

selecting the over-all inductance of the plurality of inductors by selecting at least a portion of the inductors; and

setting the over-all inductance of the plurality of inductors by having in the first state at least one switch device for which the corresponding inductor and any subsequent inductors thereof are not selected.

15. A method as defined in claim 1 wherein the aforementioned inductor is a first inductor, further comprising:

forming a plurality of inductors similar to the first inductor, each of the inductors having an inductance;

electrically connecting the inductors with a plurality of switch devices, each switch device corresponding to one of the inductors and turning off the corresponding inductor when in a first state and turning on the corresponding inductor when in a second state, each of the inductors adding to an over-all inductance of the plurality of inductors when turned on;

selecting the over-all inductance of the plurality of inductors by selecting at least a portion of the inductors; and

setting the over-all inductance of the plurality of inductors by having in the first state any switch devices that correspond to any inductors that are not selected and having in the second state any switch devices that correspond to any inductors that are selected.

16. An integrated circuit comprising:

conductor layers arranged substantially parallel to a plane of the integrated circuit;

insulating layers disposed between the conductor layers; and

an inductor formed within the conductor layers and the insulating layers and having magnetic flux lines substantially parallel to the plane of the integrated circuit upon operation of the integrated circuit.

17. An integrated circuit as defined in claim 16 wherein the inductor has a substantially coil-shaped configuration.

18. An integrated circuit as defined in claim 16 wherein:

the inductor includes:

a first segment; and

a second segment electrically connected to, proximate to and spaced apart from the first segment.

19. An integrated circuit as defined in claim 18 wherein:

the first segment of the inductor has a coil-shape in a first spiraling angular direction; and

the second segment of the inductor has a coil-shape in a second spiraling angular direction.

20. An integrated circuit as defined in claim 18 wherein:

the first segment of the inductor has a magnetic flux field in a predetermined orientation upon operation of the integrated circuit; and

the second segment of the inductor has a magnetic flux field in the predetermined orientation upon operation of the integrated circuit.

21. An integrated circuit as defined in claim 18 further comprising:

other electronic components disposed under the conductor layers and the insulating layers; and

electrical conductors disposed in the conductor layers between the first segment and second segment of the inductor, the electrical conductors electrically connecting the other electronic components.

22. An integrated circuit as defined in claim 18 further comprising:

an electrical conductor disposed in only one of the conductor layers and electrically connecting the first segment and the second segment.

23. An integrated circuit as defined in claim 16 further comprising:

a plurality of segments of the inductor; and

a plurality of electrical connectors electrically connecting the segments.

24. An integrated circuit as defined in claim 16 further comprising:

an edge of the integrated circuit; and wherein:

the inductor includes an end; and

the end of the inductor is proximate to the edge of the integrated circuit.

25. An integrated circuit as defined in claim 24 wherein the aforementioned edge of the integrated circuit is a first edge, and the aforementioned end of the inductor is a first end, further comprising:

a second edge of the integrated circuit opposite the first edge; and wherein:

the inductor includes a second end opposite the first end;

the first end of the inductor is proximate to the first edge of the integrated circuit; and

the second end of the inductor is proximate to the second edge of the integrated circuit.

26. An integrated circuit as defined in claim 24 wherein:

the magnetic flux lines of the inductor have a greatest density at the end of the inductor proximate to the edge of the integrated circuit upon operation of the integrated circuit.

27. An integrated circuit as defined in claim 16 wherein:

the inductor has a substantially rectangular cross section;

the inductor includes horizontal legs and vertical legs;

the horizontal legs are disposed within the conductor layers; and

the vertical legs are disposed within the conductor layers and the insulating layers.

28. An integrated circuit as defined in claim 16 wherein the aforementioned inductor is a first inductor, further comprising:

a second inductor formed within the conductor layers and the insulating layers and having magnetic flux lines substantially parallel to the plane of the integrated circuit upon operation of the integrated circuit, the second inductor

being substantially similar to the first inductor and offset laterally and longitudinally from the first inductor.

29. An integrated circuit as defined in claim 16 wherein the aforementioned inductor is a first inductor, further comprising:

a plurality of inductors similar to the first inductor and including an initial inductor and a last inductor, each of the inductors having an inductance, the inductors being connected in a series in which each inductor, except the last inductor in the series, is followed by at least one inductor subsequent thereto and each inductor, except the initial inductor in the series, is preceded by at least one of the inductors; and

a plurality of switch devices electrically connected to the inductors, each switch device corresponding to at least one of the inductors, each switch device turning off the corresponding inductor and any inductors subsequent to the corresponding inductor when the switch device is in a first state, each switch device turning on the corresponding inductor when the switch device and the switch devices corresponding to any inductors preceding the corresponding inductor are in a second state; and wherein:

each of the inductors adds to an over-all inductance of the plurality of inductors when turned on; and

the over-all inductance of the plurality of inductors is set by selecting at least a portion of the inductors and having in the first state at least one switch device for which the corresponding inductor and any subsequent inductors thereof are not selected.

30. An integrated circuit as defined in claim 16 wherein the aforementioned inductor is a first inductor, further comprising:

a plurality of inductors similar to the first inductor, each of the inductors having an inductance; and

a plurality of switch devices electrically connected to the inductors, each switch device corresponding to one of the inductors and turning off the corresponding inductor when in a first state and turning on the corresponding

inductor when in a second state, and wherein:

each of the inductors adds to an over-all inductance of the plurality of inductors when turned on; and

the over-all inductance of the plurality of inductors is set by selecting at least a portion of the inductors and having in the first state any switch devices that correspond to any inductors that are not selected and having in the second state any switch devices that correspond to any inductors that are selected.